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APR 11 2002
PATENT & TRADEMARK OFFICE

#4

Our Ref. No.: 042390.P12921

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:)
)
Alankar Saxena, et al.)
)
Serial No. 10/033,439)
)
Filing Date: December 28, 2001)
)
For: DUAL MEMORY CHANNEL INTERLEAVING)
FOR GRAPHICS AND MPEG)

SUBMISSION OF FORMAL DRAWINGS

Hon. Commissioner of Patents and Trademarks
Washington, D.C. 20231

Dear Sir:

Submitted herewith are formal drawings, Figures 1-14.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

Dated: 4/29/02

Eric S. Hyman, Reg. No. 30,139

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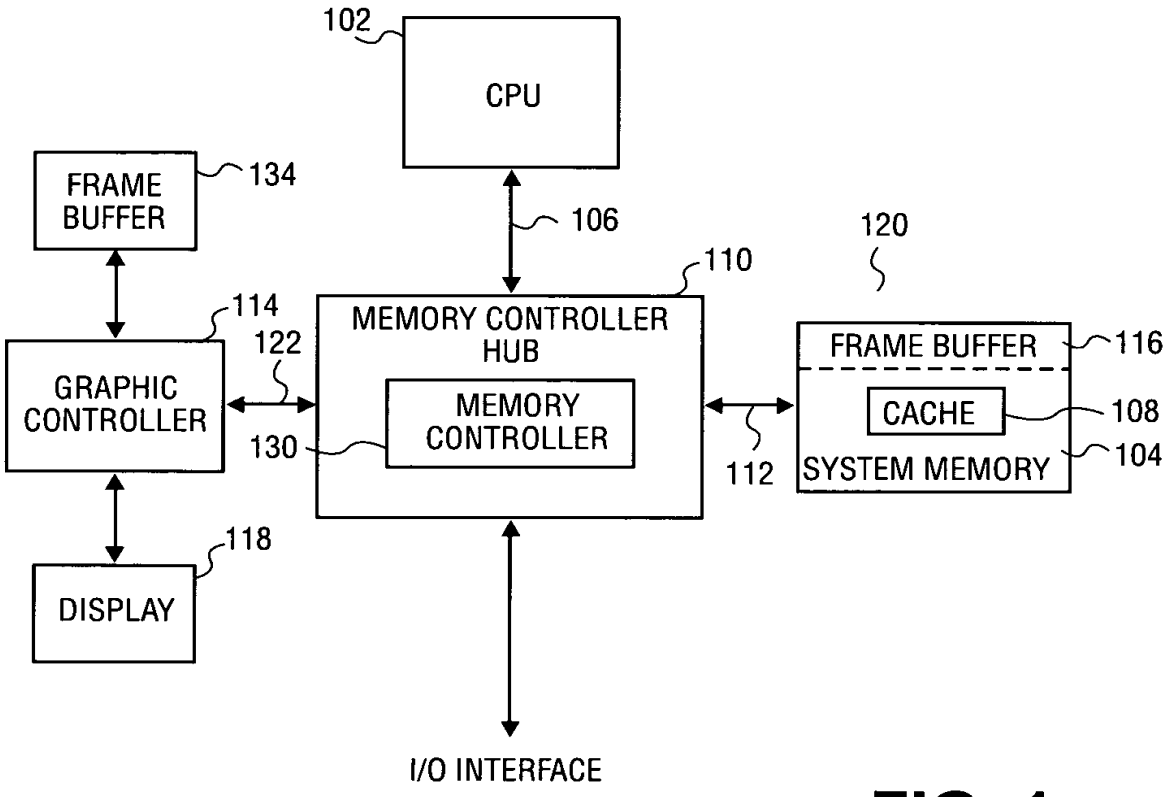
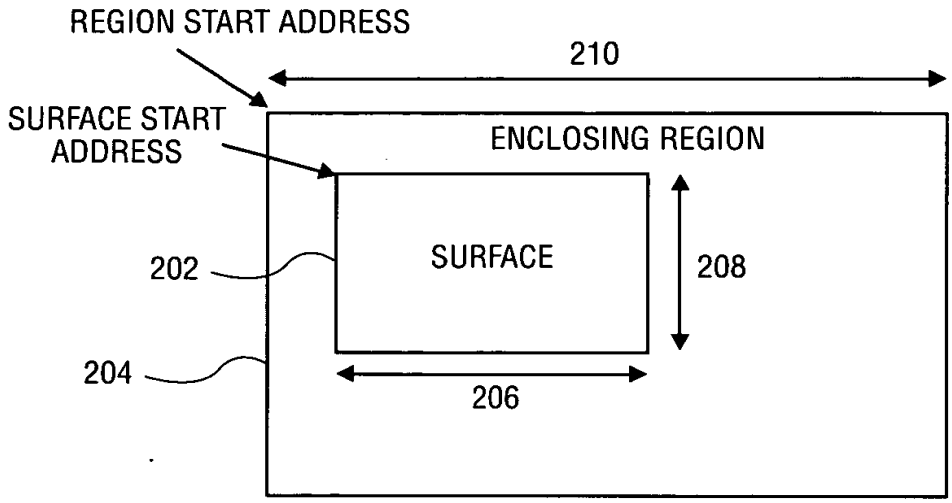

102
CPU
FRAME BUFFER
134
106
120
110
114
122
MEMORY CONTROLLER HUB
FRAME BUFFER
116
GRAPHIC CONTROLLER
MEMORY CONTROLLER
CACHE
108
130
112
SYSTEM MEMORY
104
118
DISPLAY
I/O INTERFACE

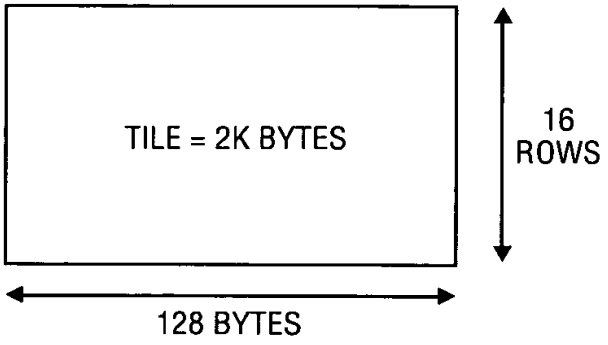
FIG. 1

100



200

FIG. 2A



212

FIG. 2B

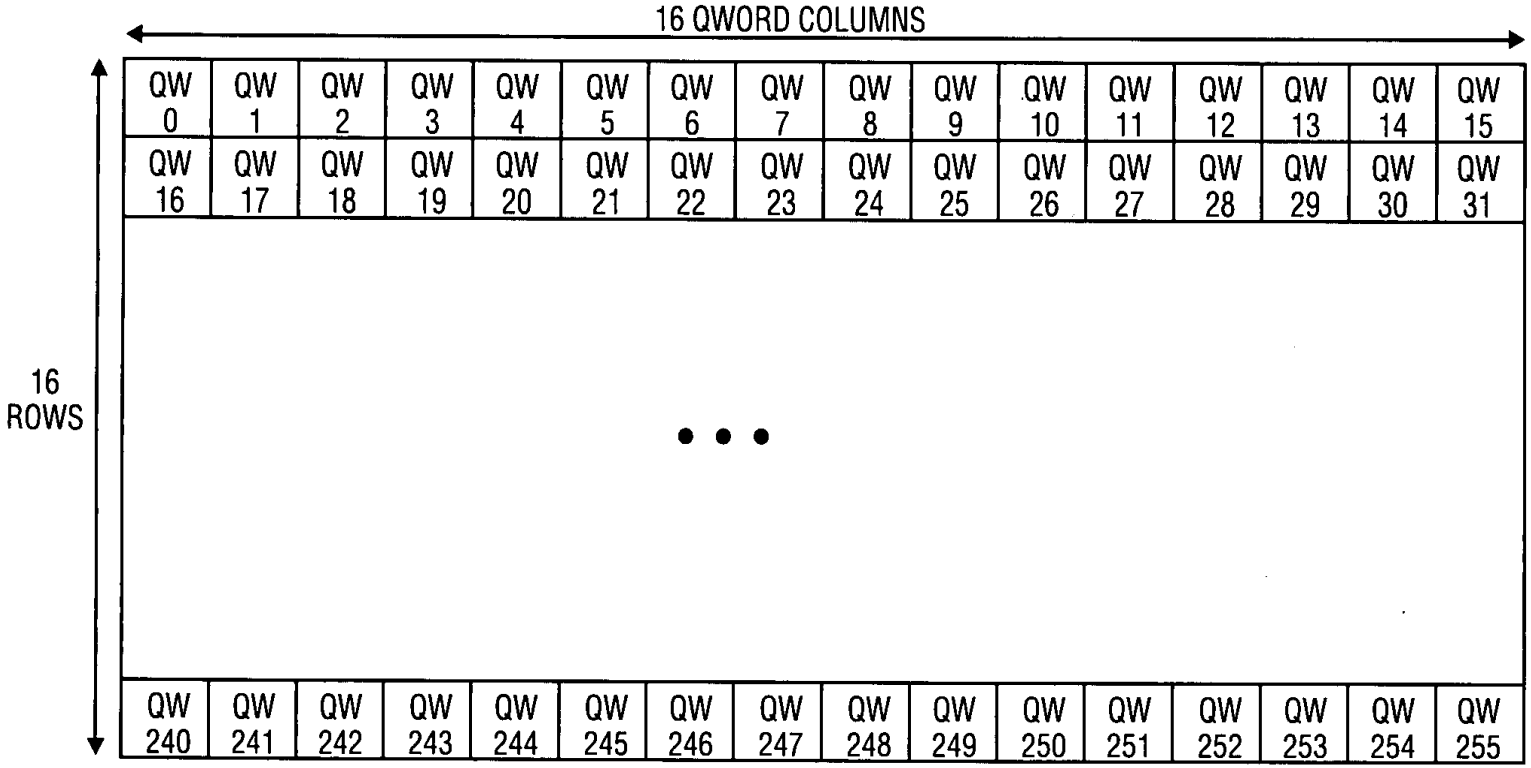

16 QWORD COLUMNS
16 ROWS
QW 0
QW 1
QW 2
QW 3
QW 4
QW 5
QW 6
QW 7
QW 8
QW 9
QW 10
QW 11
QW 12
QW 13
QW 14
QW 15
QW 16
QW 17
QW 18
QW 19
QW 20
QW 21
QW 22
QW 23
QW 24
QW 25
QW 26
QW 27
QW 28
QW 29
QW 30
QW 31
QW 240
QW 241
QW 242
QW 243
QW 244
QW 245
QW 246
QW 247
QW 248
QW 249
QW 250
QW 251
QW 252
QW 253
QW 254
QW 255

FIG. 3

300

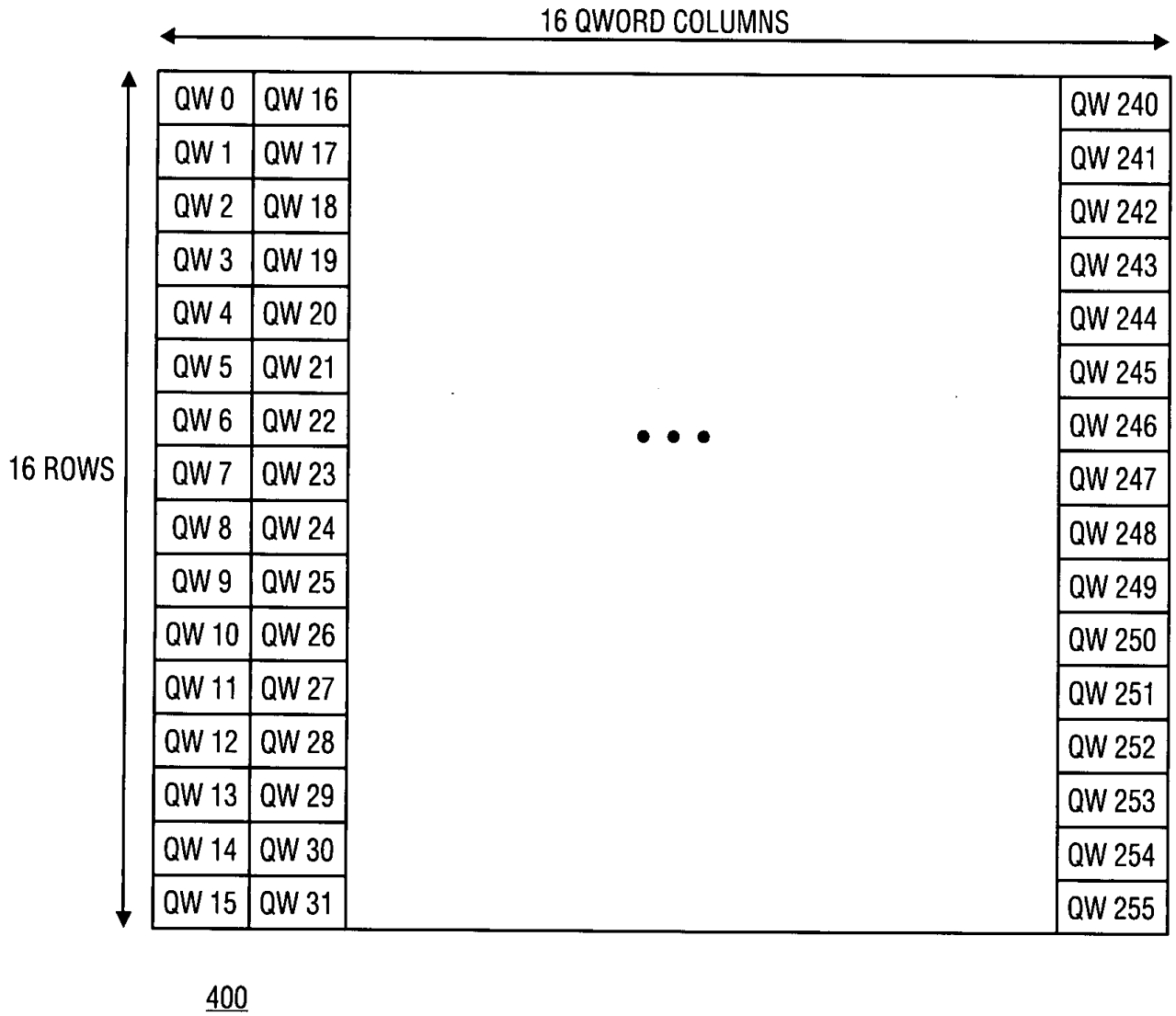

16 QWORD COLUMNS
16 ROWS
QW 0
QW 16
QW 1
QW 17
QW 2
QW 18
QW 3
QW 19
QW 4
QW 20
QW 5
QW 21
QW 6
QW 22
QW 7
QW 23
QW 8
QW 24
QW 9
QW 25
QW 10
QW 26
QW 11
QW 27
QW 12
QW 28
QW 13
QW 29
QW 14
QW 30
QW 15
QW 31
QW 240
QW 241
QW 242
QW 243
QW 244
QW 245
QW 246
QW 247
QW 248
QW 249
QW 250
QW 251
QW 252
QW 253
QW 254
QW 255
400

FIG. 4

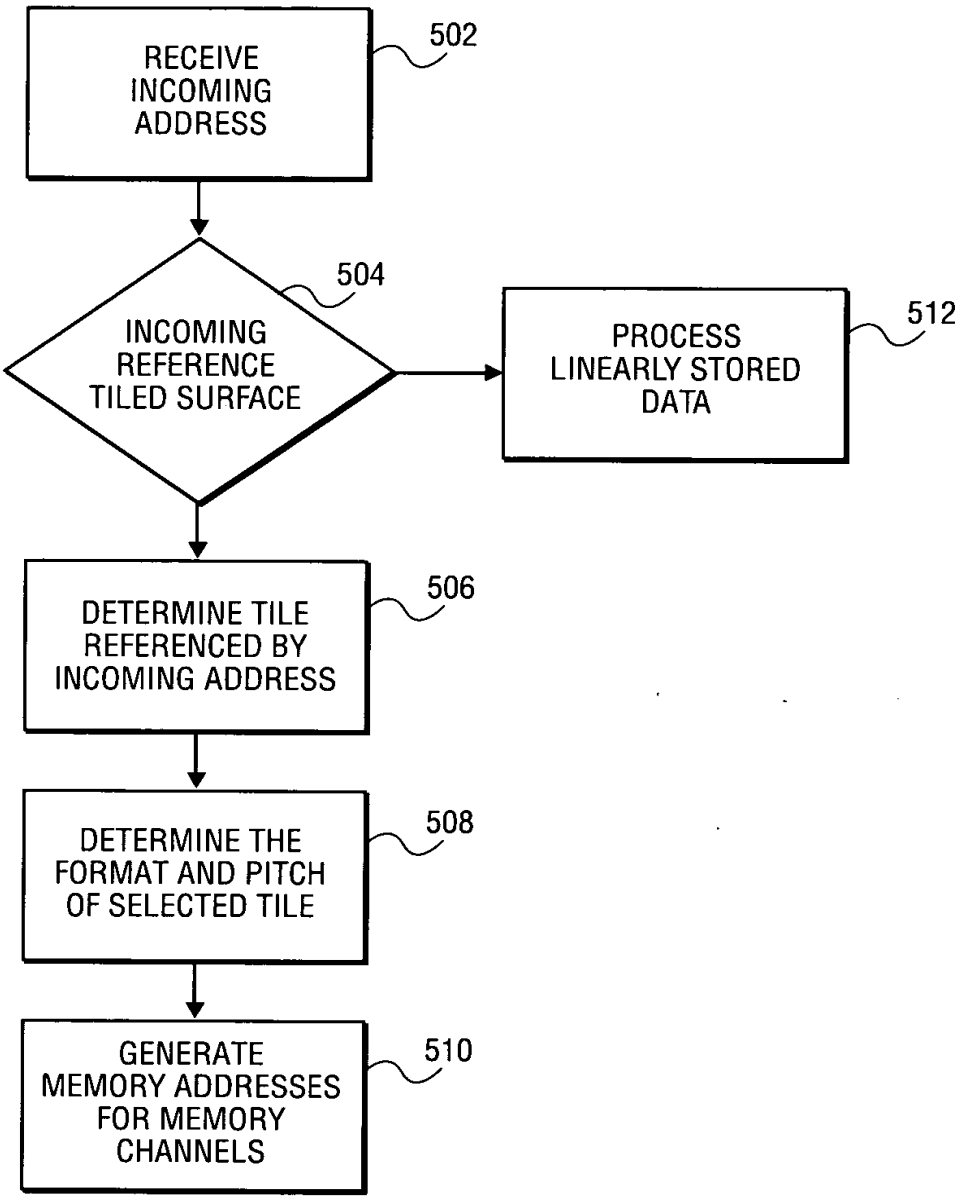

RECEIVE INCOMING ADDRESS
502
INCOMING REFERENCE TILED SURFACE
504
PROCESS LINEARLY STORED DATA
512
DETERMINE TILE REFERENCED BY INCOMING ADDRESS
506
DETERMINE THE FORMAT AND PITCH OF SELECTED TILE
508
GENERATE MEMORY ADDRESSES FOR MEMORY CHANNELS
510

FIG. 5

500

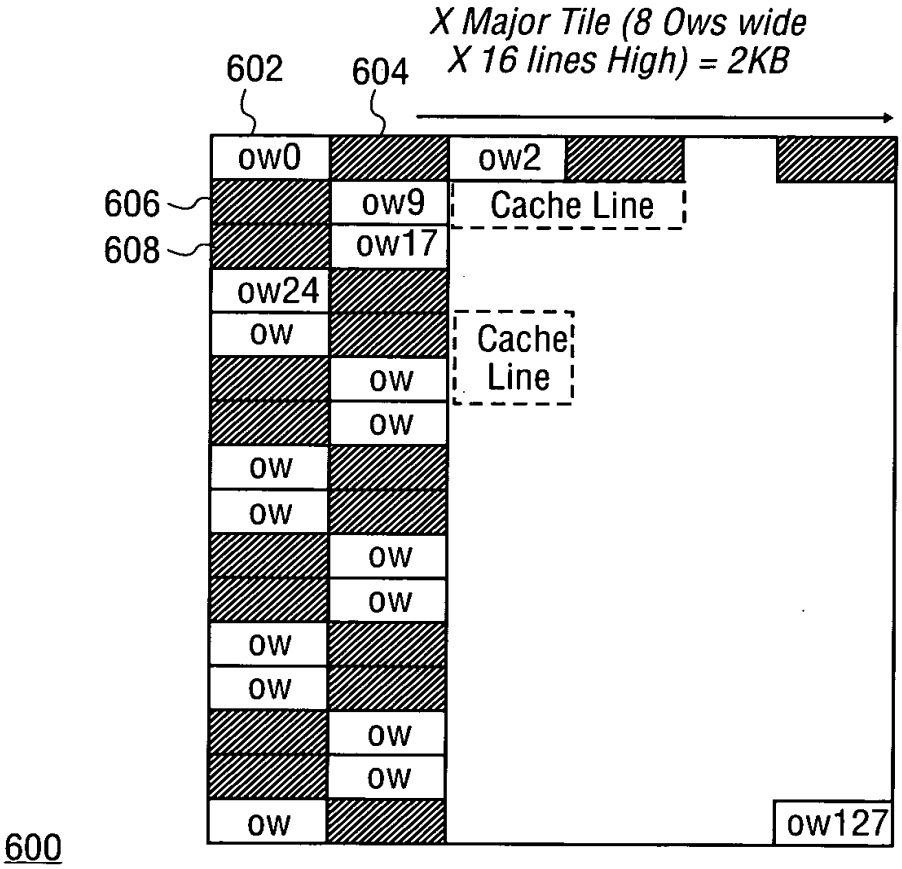
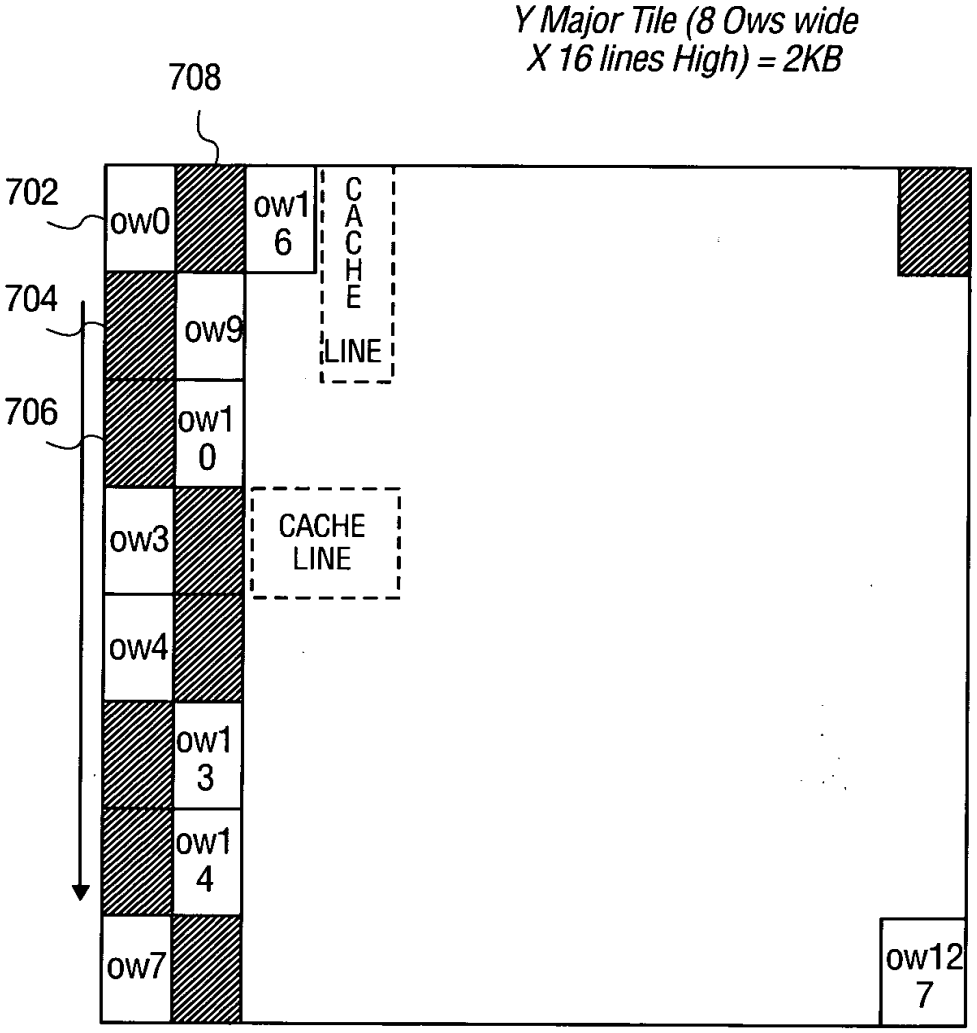

X Major Tile (8 Ows wide
X 16 lines High) = 2KB
602
604
606
608
ow0
ow2
ow9
Cache Line
ow17
ow24
ow
Cache
Line
ow127
600

FIG. 6


Y Major Tile (8 Ows wide
X 16 lines High) = 2KB
708
702
704
706
ow0
ow1
6
CACHE
LINE
ow9
ow1
0
ow3
CACHE
LINE
ow4
ow1
3
ow1
4
ow7
ow12
7

700

FIG. 7

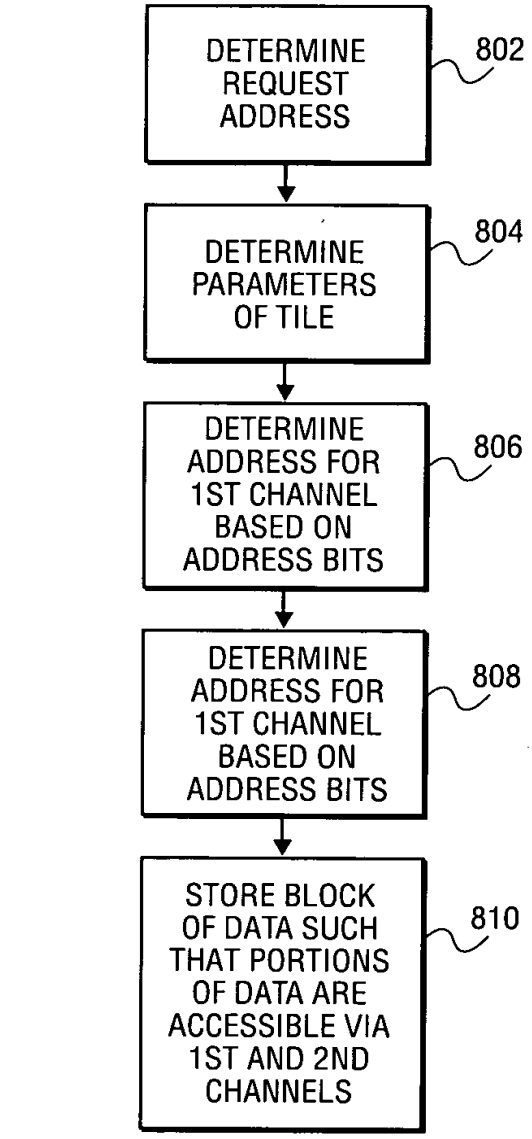

DETERMINE REQUEST ADDRESS
802
DETERMINE PARAMETERS OF TILE
804
DETERMINE ADDRESS FOR 1ST CHANNEL BASED ON ADDRESS BITS
806
DETERMINE ADDRESS FOR 1ST CHANNEL BASED ON ADDRESS BITS
808
STORE BLOCK OF DATA SUCH THAT PORTIONS OF DATA ARE ACCESSIBLE VIA 1ST AND 2ND CHANNELS
810

FIG. 8

800

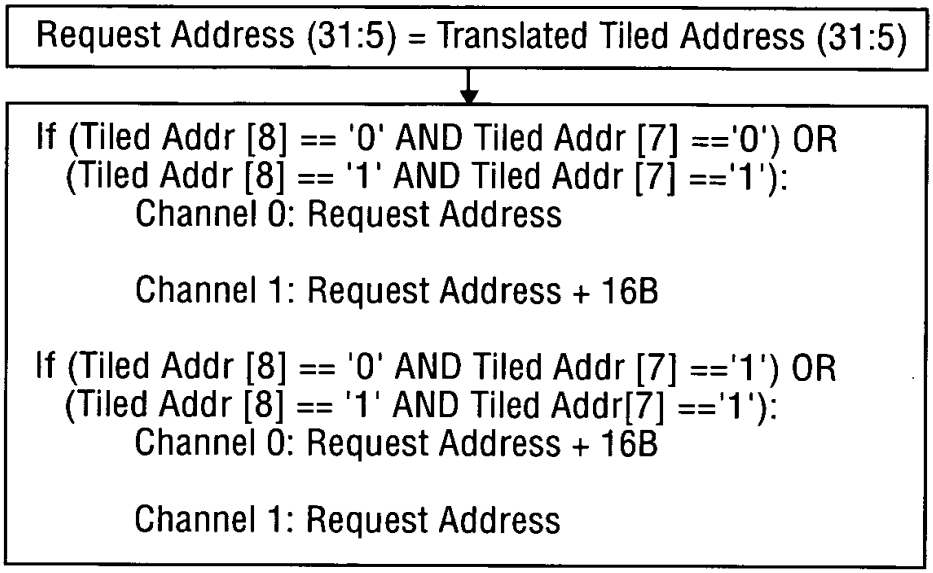

Request Address (31:5) = Translated Tiled Address (31:5)
If (Tiled Addr [8] == '0' AND Tiled Addr [7] =='0') OR
(Tiled Addr [8] == '1' AND Tiled Addr [7] =='1'):
Channel 0: Request Address
Channel 1: Request Address + 16B
If (Tiled Addr [8] == '0' AND Tiled Addr [7] =='1') OR
(Tiled Addr [8] == '1' AND Tiled Addr[7] =='1'):
Channel 0: Request Address + 16B
Channel 1: Request Address

FIG. 9

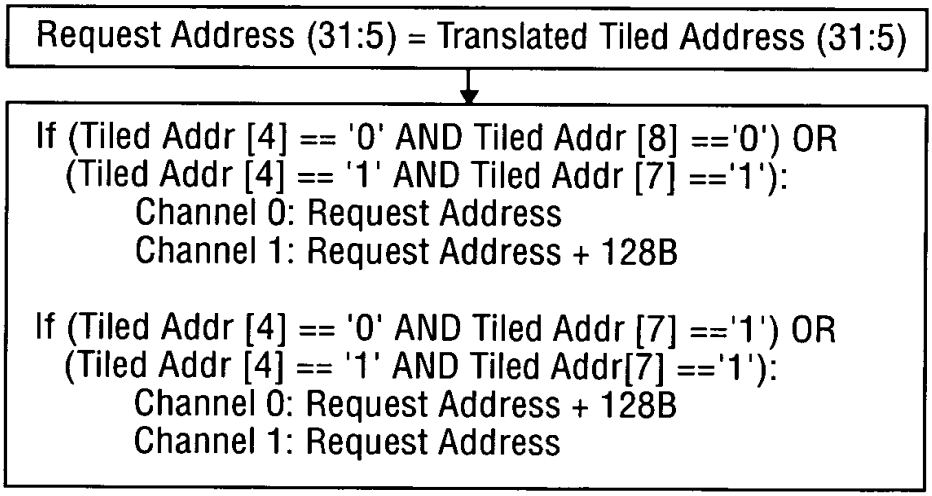

Request Address (31:5) = Translated Tiled Address (31:5)
If (Tiled Addr [4] == '0' AND Tiled Addr [8] =='0') OR
(Tiled Addr [4] == '1' AND Tiled Addr [7] =='1'):
Channel 0: Request Address
Channel 1: Request Address + 128B
If (Tiled Addr [4] == '0' AND Tiled Addr [7] =='1') OR
(Tiled Addr [4] == '1' AND Tiled Addr[7] =='1'):
Channel 0: Request Address + 128B
Channel 1: Request Address

FIG. 10

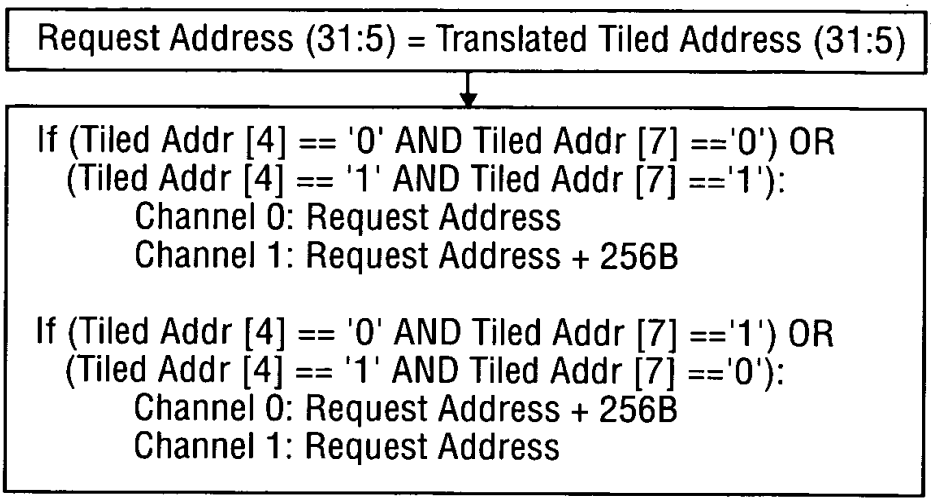

Request Address (31:5) = Translated Tiled Address (31:5)
If (Tiled Addr [4] == '0' AND Tiled Addr [7] =='0') OR
(Tiled Addr [4] == '1' AND Tiled Addr [7] =='1'):
Channel 0: Request Address
Channel 1: Request Address + 256B
If (Tiled Addr [4] == '0' AND Tiled Addr [7] =='1') OR
(Tiled Addr [4] == '1' AND Tiled Addr [7] =='0'):
Channel 0: Request Address + 256B
Channel 1: Request Address

FIG. 11

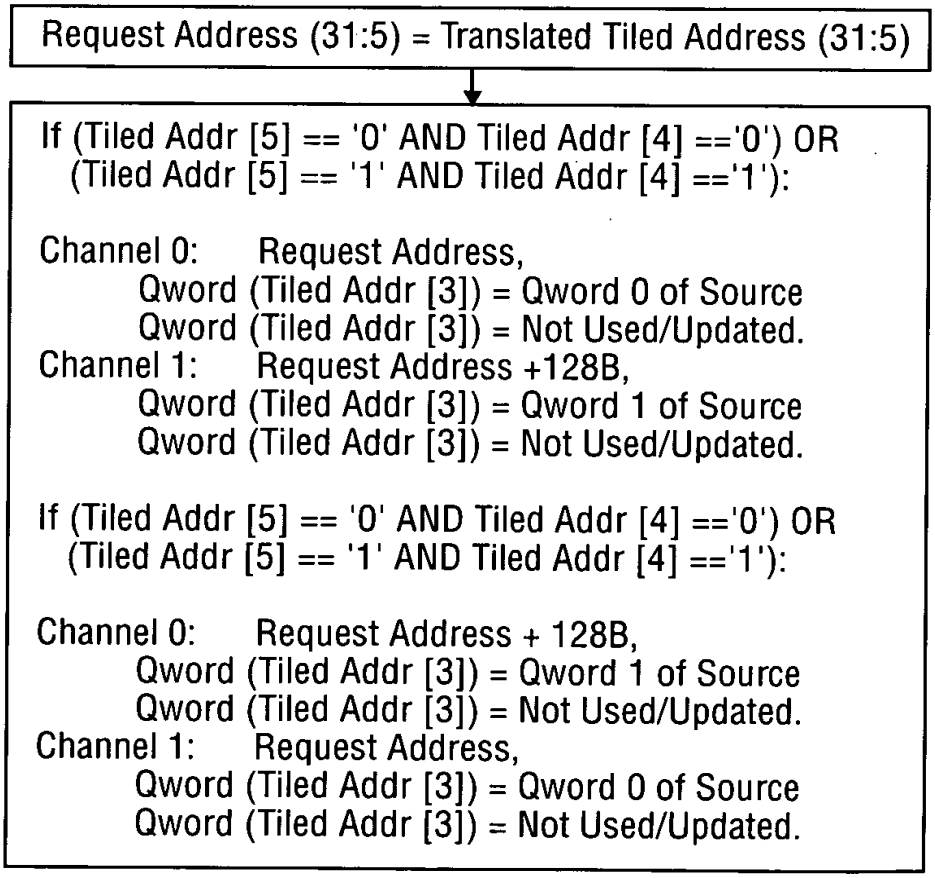

Request Address (31:5) = Translated Tiled Address (31:5)
If (Tiled Addr [5] == '0' AND Tiled Addr [4] =='0') OR
(Tiled Addr [5] == '1' AND Tiled Addr [4] =='1'):
Channel 0: Request Address,
Qword (Tiled Addr [3]) = Qword 0 of Source
Qword (Tiled Addr [3]) = Not Used/Updated.
Channel 1: Request Address +128B,
Qword (Tiled Addr [3]) = Qword 1 of Source
Qword (Tiled Addr [3]) = Not Used/Updated.
If (Tiled Addr [5] == '0' AND Tiled Addr [4] =='0') OR
(Tiled Addr [5] == '1' AND Tiled Addr [4] =='1'):
Channel 0: Request Address + 128B,
Qword (Tiled Addr [3]) = Qword 1 of Source
Qword (Tiled Addr [3]) = Not Used/Updated.
Channel 1: Request Address,
Qword (Tiled Addr [3]) = Qword 0 of Source
Qword (Tiled Addr [3]) = Not Used/Updated.

FIG. 12

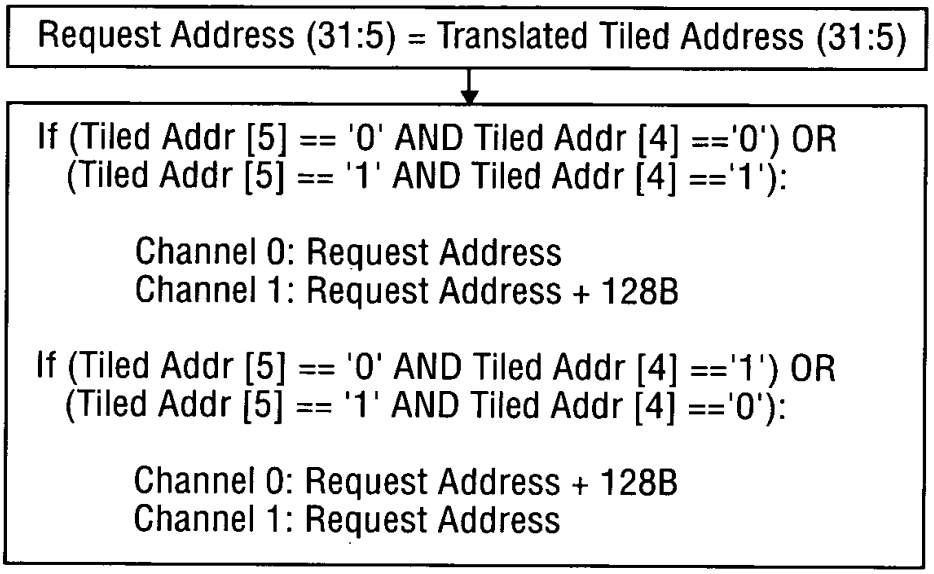

Request Address (31:5) = Translated Tiled Address (31:5)
If (Tiled Addr [5] == '0' AND Tiled Addr [4] =='0') OR
(Tiled Addr [5] == '1' AND Tiled Addr [4] =='1'):
Channel 0: Request Address
Channel 1: Request Address + 128B
If (Tiled Addr [5] == '0' AND Tiled Addr [4] =='1') OR
(Tiled Addr [5] == '1' AND Tiled Addr [4] =='0'):
Channel 0: Request Address + 128B
Channel 1: Request Address

FIG. 13

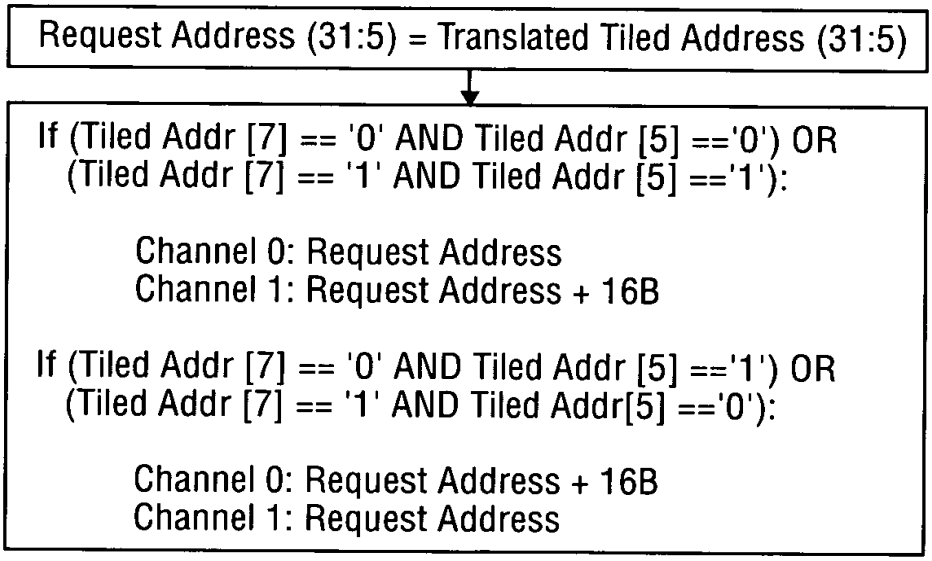

Request Address (31:5) = Translated Tiled Address (31:5)
If (Tiled Addr [7] == '0' AND Tiled Addr [5] =='0') OR
(Tiled Addr [7] == '1' AND Tiled Addr [5] =='1'):
Channel 0: Request Address
Channel 1: Request Address + 16B
If (Tiled Addr [7] == '0' AND Tiled Addr [5] =='1') OR
(Tiled Addr [7] == '1' AND Tiled Addr[5] =='0'):
Channel 0: Request Address + 16B
Channel 1: Request Address

FIG. 14